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Second Quarterly Report

for

PHOTON-COUPLED ISOLATION SWITCH

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ABSTRACT

Optoelectronic techniques are being used in the development of a new type of photon-coupled integrated circuit. This device functions as an isolation switch by providing a transistor output electrically isolated from the driving sources and all other terminals of the switch. The isolation switch combines a monolithic silicon integrated driver circuit, a gallium arsenide photo emitting diode and a silicon phototransistor. In operation, the driver circuit supplies bias for the GaAs diode, and the phototransistor, optically coupled to the GaAs diode, acts as the ouput transistor switch.

The development program is divided into two phases:

Phase I, design and breadboarding of the driver circuit and development of the gallium arsenide emitting diode-silicon phototransistor pair.

Phase II, integration of the driver circuit and prototype production of the complete isolation switch.

In the first quarter of the program under Phase I, the design and breadboarding of the driver circuit was completed. The silicon phototransistor was also designed and diffusion masks produced.

During the second quarter, phototransistors satisfying the current gain and breakdown voltage requirements were fabricated. Gallium Arsenide Switches, which combined emitting diodes with the phototransistors, also satisfied the design objectives for coupling efficiency. Modification of the phototransistor is in process to eliminate inversion layer effects found in the present structure.

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SECTION I

INTRODUCTION

Transformers are widely used in discrete electronic circuits for the function of isolation. Four-terminal operation, such as obtained with a transformer, provides the capability of coupling signals between circuits operating at different d-c potentials and also of minimizing ground-loop currents such as produced with direct connections. Unfortunately, the transformer function cannot be effectively provided with the conventional techniques used in integrated circuits. Successful means for obtaining isolation in integrated circuits has been achieved, however, by incorporating a solid-state light emitter-detector pair. Most efficient signal coupling between the pair is obtained using a GaAs P-N junction photo emitting diode with a Si P-N junction detector. Several types of optoelectronic devices using this source-detector system have been developed.[1, 2] These include an isolated input transistor, an isolated-gate P-N-P-N-Type switch, a multiplex switch that does not require a driving transformer, and an isolated-input pulse amplifier.

In the present contract, the technique of using a photon-coupled pair is used in the development of a new type of integrated circuit switch. This photon-coupled isolation switch is a three-chip device combining a monolithic Si driver circuit, a GaAs emitting diode, and a Si phototransistor. Input to the isolation switch is applied to the driver circuit which supplies bias to the GaAs diode. The phototransistor is optically coupled to the emitting diode and is electrically isolated from the driving sources and the other terminals of the switch. The development program is divided into two phases. In Phase I, the driver circuit is designed using data from elements similar to those to be used in the integrated switch and the emitting diode-phototransistor pair (GaAs Switch) is developed. In Phase II, the driver circuit is integrated in a monolithic Si wafer and the three chips (driver, emitting diode, and photo-transistor) are combined in a miniature integrated circuit package to form the complete isolation switch.

In the first quarter of the program under Phase I, detailed characterization of the isolated-input optoelectronic pulse amplifier, Texas Instruments type SNX1304 was performed. Integration of the driver circuit in Phase II is to be made using the same diffusion processes as used for this device. Design and breadboarding of the driver circuit were also substantially completed. The phototransistor was designed and diffusion masks were produced.

Work performed during the second quarter of the contract under Phase I are described in this report. Phototransistors having the desired current gain and breakdown

voltage characteristics were successfully fabricated. Optical coupling of the emitter-detector pair were also as desired. Measurements of high temperature leakage for the phototransistor revealed the formation of inversion layers on the surface of the transistor which should be eliminated with modifications in process.

SECTION II

TECHNICAL DISCUSSION

A. PHOTOTRANSISTOR FABRICATION

Phototransistors fulfilling the design requirements for current gain and breakdown voltage were successfully produced. With base widths adjusted to obtain a nominal H_{FE} of 500, the H_{FE} distribution was largely between 450 and 700.

B. TRANSISTOR PRELIMINARY EVALUATION

Initial data for eight GaAs Switches (emitter diode-phototransistor pair) are given in Table I. These consist of the transistor collector-emitter breakdown BV_{CEO} and leakage current I_{CEO}. Also given are the collector current $I_{C(W.C.)}$, and transistor saturation voltage current $V_{CE(sat)}$, both for an emitter diode current equal to the worst-case minimum value. All of these devices meet the requirements for BV_{CEO} greater than 35 V, $I_{C(W.C.)}$ greater than 10 mA and $V_{CE(sat)}$ less than 0.6 V. Six of the devices meet the I_{CEO} requirements (less than 0.1 μA and 20 μA at 25°C and 100°C, respectively).

For a number of units the photo-induced current in the phototransistor was measured by shorting the collector and emitter terminals, and measuring the short-circuit current between this connection and the base lead (brought out for Phase I devices). Initial results for two types of GaAs emitter diodes are shown in Table II. The first group (units 2 through 13) used GaAs emitters having outputs which range from "average" to "excellent". The second group used GaAs emitters with "poor" outputs. The latter GaAs emitters were not considered good enough for Phase I devices, but were tested to obtain reference values. The data shown was measured at 25°C. A good estimate for the efficiency of the GaAs emitter at 100°C is 1/2 the 25°C value. For the first group of GaAs emitters, the half-values range from 40 to 75 μA, and for the second group, 16 to 20 μA. These values are comparable to the range of 20 to 40 μA assumed in the first quarterly report[3] for average GaAs diodes.

C. TRANSISTOR LEAKAGE EFFECTS

Further evaluation of the leakage characteristics of the phototransistor revealed effects which result in a large collector-emitter leakage. One source of leakage was traced to the epoxy encapsulation. This epoxy had been used for the SNX1304 without difficulty and was being considered for use in the GaAs Switch. In the case of the phototransistor, it was found that the leakage current at 100°C was excessive for units in which the epoxy also contacted the base metallization. Leakage for devices with

Table I. Initial Data For GaAs Emitter Diode — Si Phototransistor Pair

Unit No.	BV_{CEO} (V) I_C = 100 μA		I_{CEO} (μA) V_{CE} = 20 V		$I_{C(WC)}$ (mA) I_D = 22 mA V_{CE} = 0.6 V T = 100°C	$V_{CE(sat)}$ (V) I_D = 22 mA I_C = 10 mA T = 100°C
	T = 25°C	T = 100°C	T = 25°C	T = 100°C		
1	79	68	0.16	24	13	0.31
2	77	74	0.03	9.6	21	0.24
3	85	84	0.02	3.9	35	0.17
4	81	76	0.06	14	29	0.21
5	84	83	0.03	5.4	24	0.21
6	76	72	0.03	5.7	21	0.22
7	84	74	0.02	2.8	26	0.19
8	78	52	0.07	22	26	0.23

Table II. Photo-induced Current in Phototransistor

I_D = 22 mA
T = 25°C

Unit No.	I_X (μA)	1/2 I_X (μA)
2	143	71
3	85	42
7	87	43
8	80	40
10	118	59
11	108	54
13	150	75
A1	32	16
A2	32	16
A3	40	20
A4	34	16

and without the epoxy contacting the metallization are given in Table III. Increases in the conductivity of the epoxy with increasing temperature provided a resistive leakage between the collector and base leads. Using the average leakage value for the six units of 117 μA and assuming a value for H_{FE} of 500, the equivalent resistance can be calculated to be 85 megohms.

Table III. Collector-emitter Leakage Current of Epoxy Encapsulated Phototransistors

$T = 100°C$

I_{CE} at $V_{CE} = 20$ V

BV_{CEO} at $I_C = 100$ μA

Epoxy Contacting Base			Epoxy Not Contacting Base		
Unit No.	I_{CEO} (μA)	BV_{CEO} (V)	Unit No.	I_{CEO} (μA)	BV_{CEO} (V)
1	140	16	2	8	58
4	64	22	7	2	54
5	57	24	10	4	63
6	69	21	13	7	44
9	140	16			
12	230	12			

Another type of collector-emitter leakage was found which was associated with the coupling glass, high temperature and bias. This effect was only demonstrated by transistors having the GaAs emitter diode and coupling glass. This also was independent of the epoxy. This leakage effect can be described as follows: typically, if a collector to emitter bias current of 100 μA was applied for a few minutes in a 100°C ambient, the voltage drop of the unit slowly decreased from about 50 volts to about 20 volts. The time required for the total change varied greatly, and some units did not demonstrate the effect until after a few temperature cyclings. Both Ge-P-Se and Se-As-S coupling glasses were used with the same results.

In ordinary applications, the design of the transistor should be adequate; tests indicated no instability for the discrete transistor at 100°C. For the GaAs Switch, the coupled pair, characterizations of the leakage effect were made to evaluate its cause. During the leakage tests above, there was no external potential applied to the GaAs diodes and therefore no applied potential across the glass bond. It was suspected that the leakage effects were due to inversion layers on the surface of the transistor which were related

to the characteristics of the coupling glass. The effects of changing the field on the glass by varying the potential between the GaAs and Si wafers were studied. The following results for a representative GaAs switch were typical. In Figure 1, the collector-emitter breakdown voltage for the phototransistor at 100° C is given as a function of V_G, the voltage across the coupling glass. Sufficient time (1 to 10 minutes) was allowed for each value to stabilize. A pronounced effect is evident. From these results, it can be deduced, that with no connection to the GaAs wafer, the potential on the wafer initially follows that on the collector (since this covers most of the area under the GaAs diode) so that the breakdown voltage is initially high. As the potential on the GaAs wafer slowly drops due to package leakage paths, the breakdown voltage falls (as shown in Figure 1).

The leakage currents for the collector-base junction I_{CB}, for the collector-emitter junction with open base I_{CEO}, and for the collector-emitter junction with base and emitter shorted I_{CES} are given as a function of V_G in Figures 2 and 3. Transistor supply voltages of 3 and 35 volts, respectively, are used. In both figures, for $V_G \approx 30$ V, $I_{CEO} \approx H_{FE} I_{CB}$ and $I_{CES} \approx I_{CB}$, as expected. For $V_G > 50$ V, V_G has only a small effect on I_{CB}, but both I_{CEO} and I_{CES} experience rapid increases. The value of V_G for which this occurs is not dependent on the transistor supply voltage V_C. This is characteristic of an inversion layer which bridges the base, supplying a conductive path between collector and emitter.

Also in both cases, for $V_G < V_C - 20$ V all three currents increase greatly. In this region $I_{CEO} \approx H_{FE} I_{CB}$ and $I_{CES} \approx I_{CB}$. This indicates a leakage of the collector-base junction due to an inversion layer across the collector.

D. PHOTOTRANSISTOR REDESIGN

To eliminate the inversion layers, a redesign of the phototransistor is required. Diffusion outlines for the new design are shown in Figure 4; and the metallization pattern, in Figure 5. Remedies taken to eliminate the leakage effects include the addition of an N^+ diffusion (guard-ring) surrounding the base as shown in Figure 4, and a contact to the ring which completely covers the collector-base junction over the oxide field-relief electrode in Figure 5. These modifications should prevent contact to the base of a collector inversion layer. The base surface concentration is also being increased to reduce the probability of formation of an inversion layer on the base. The field-relief electrode should also prevent a base inversion layer from contacting the collector, which eliminates its effect on leakage current.

E. NOISE TRANSMISSIBILITY

Noise transmissibility, is defined by the signal amplitude at the collector of the transistor under nonconducting conditions for 5 V pulses applied at the emitter terminal. As described in the first quarterly report, noise transmissibility is related only to the P-N junction capacitances of the transistor, and the capacitances of the circuit

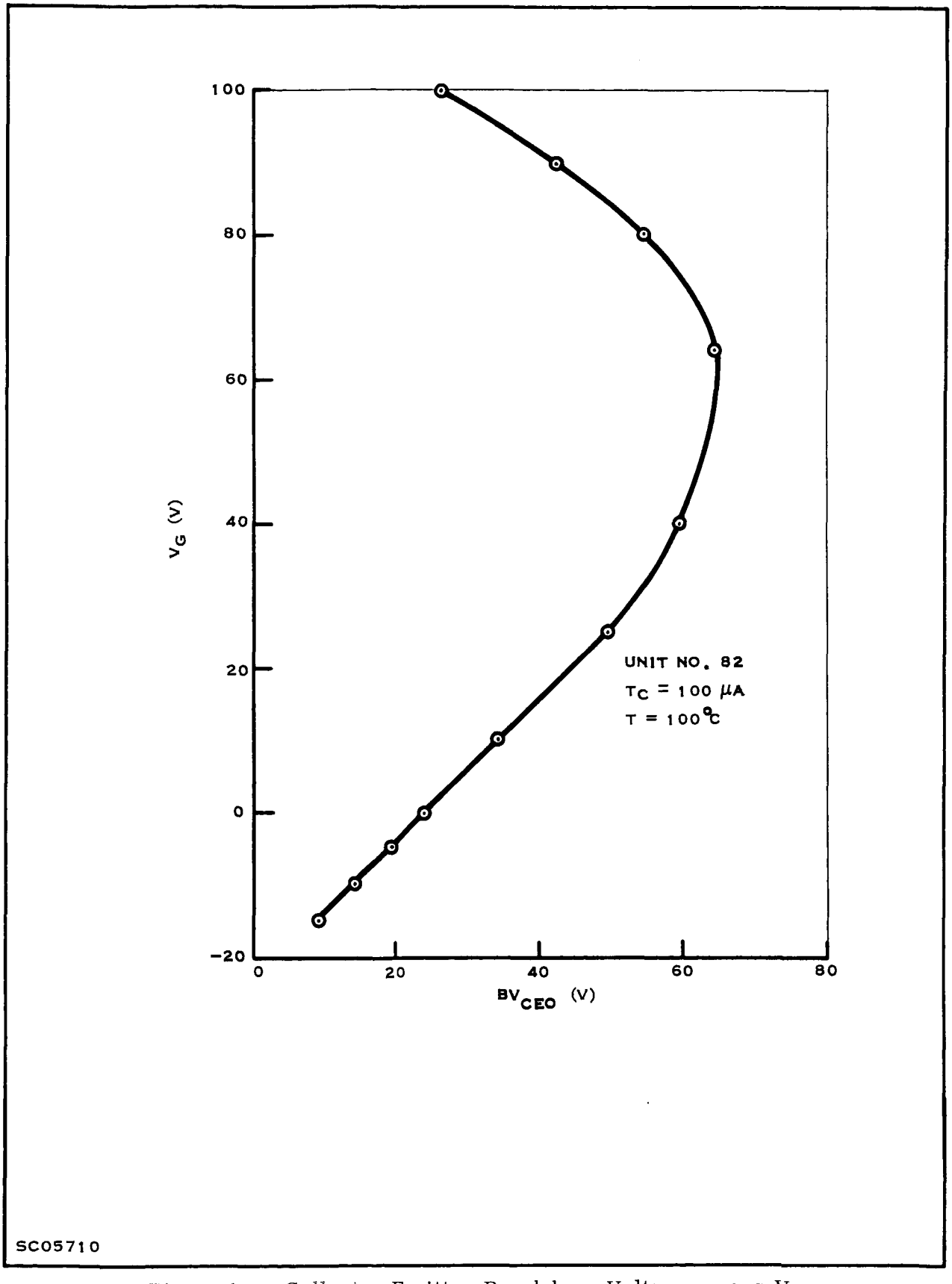

Figure 1. Collector Emitter Breakdown Voltage versus V_G

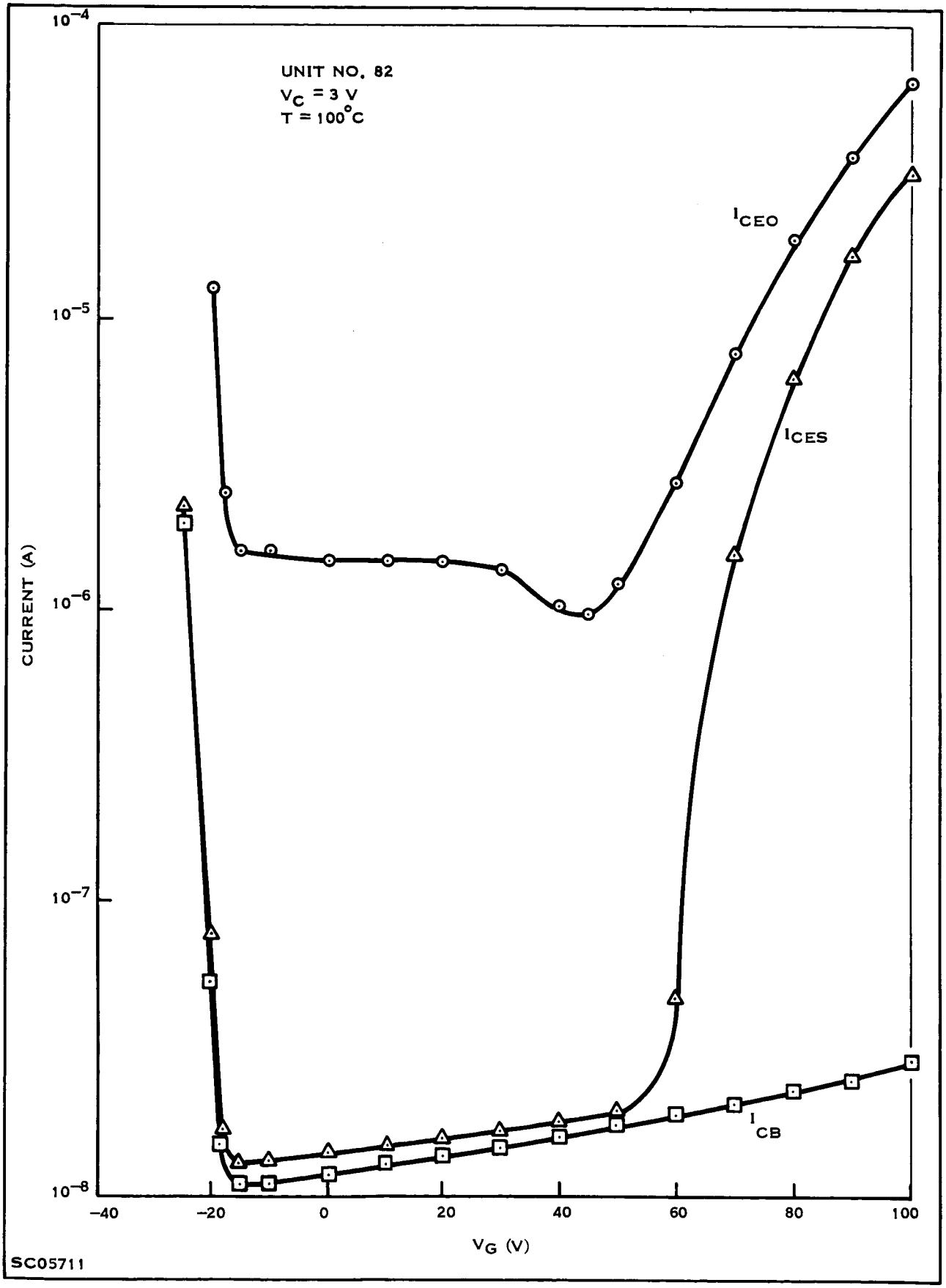

Figure 2. Transistor Leakage Currents versus V_G (V_C = 3 Volts)

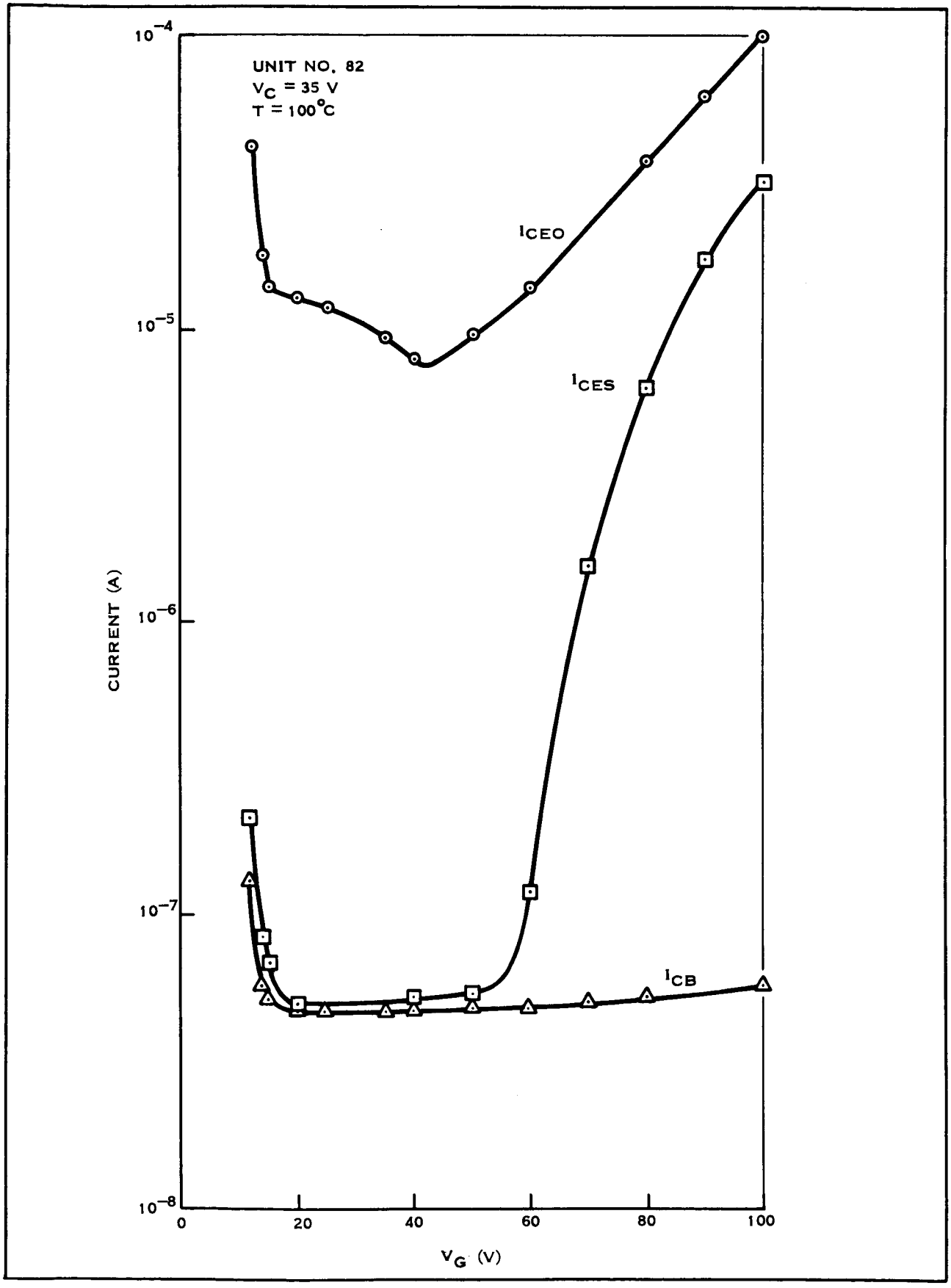

Figure 3. Transistor Leakage Currents versus V_G (V_C = 35 Volts)

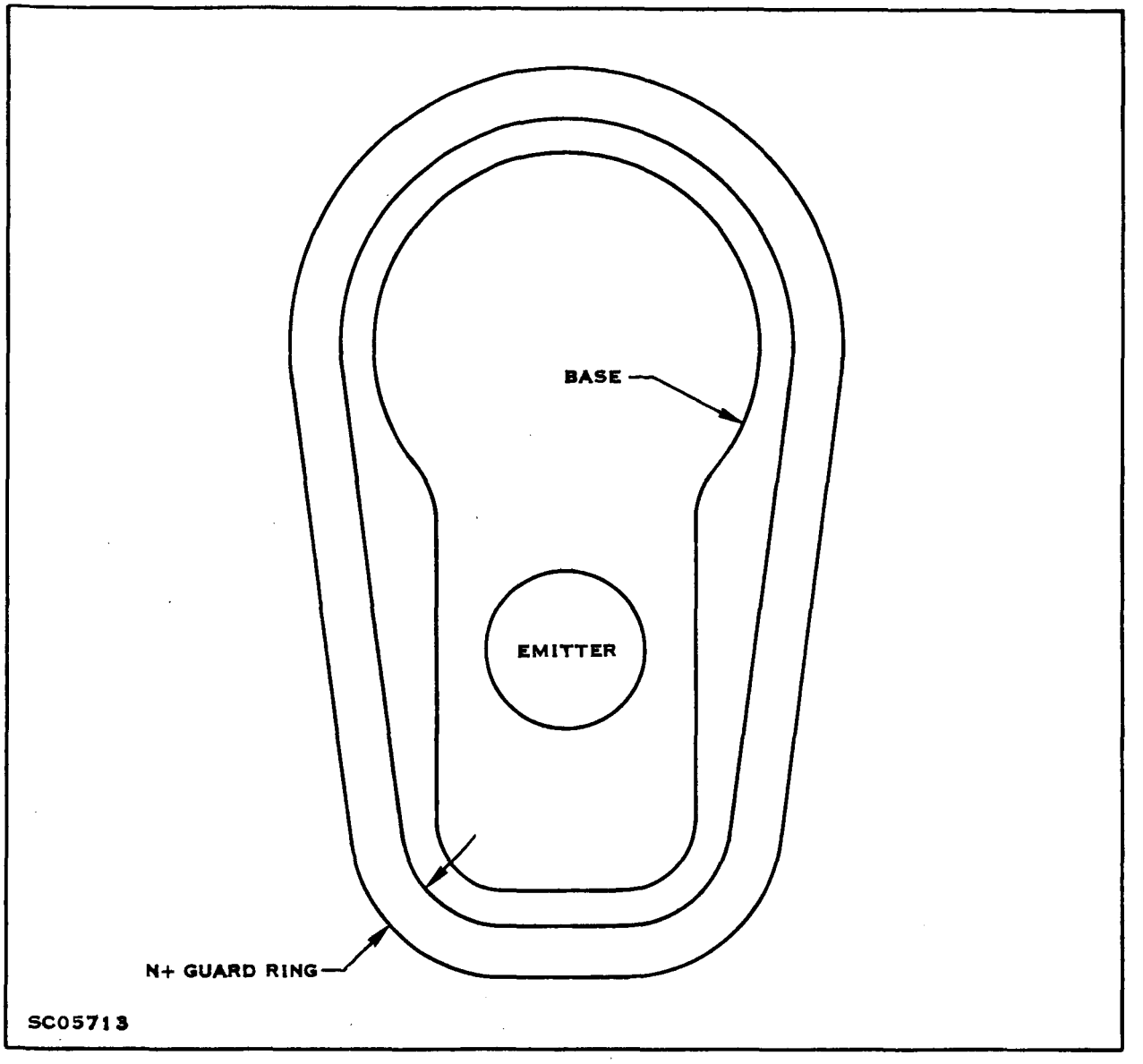

Figure 4. Phototransistor Diffusion Layout

components and the measuring jig. Values obtained for present devices, with the GaAs diode connected to ground, were measured to be about 1.4 to 1.6 V, compared to the maximum specification of 2 V.

Noise transmissibility should be greater with the new design. The base area was increased by 9%, producing a corresponding increase in the base capacitance. Also the increase in base concentration increases the emitter capacitance. To compensate for these effects, the emitter area was reduced by 20%, reducing the base-emitter capacitance at the expense of a slightly greater collector-emitter saturation voltage.

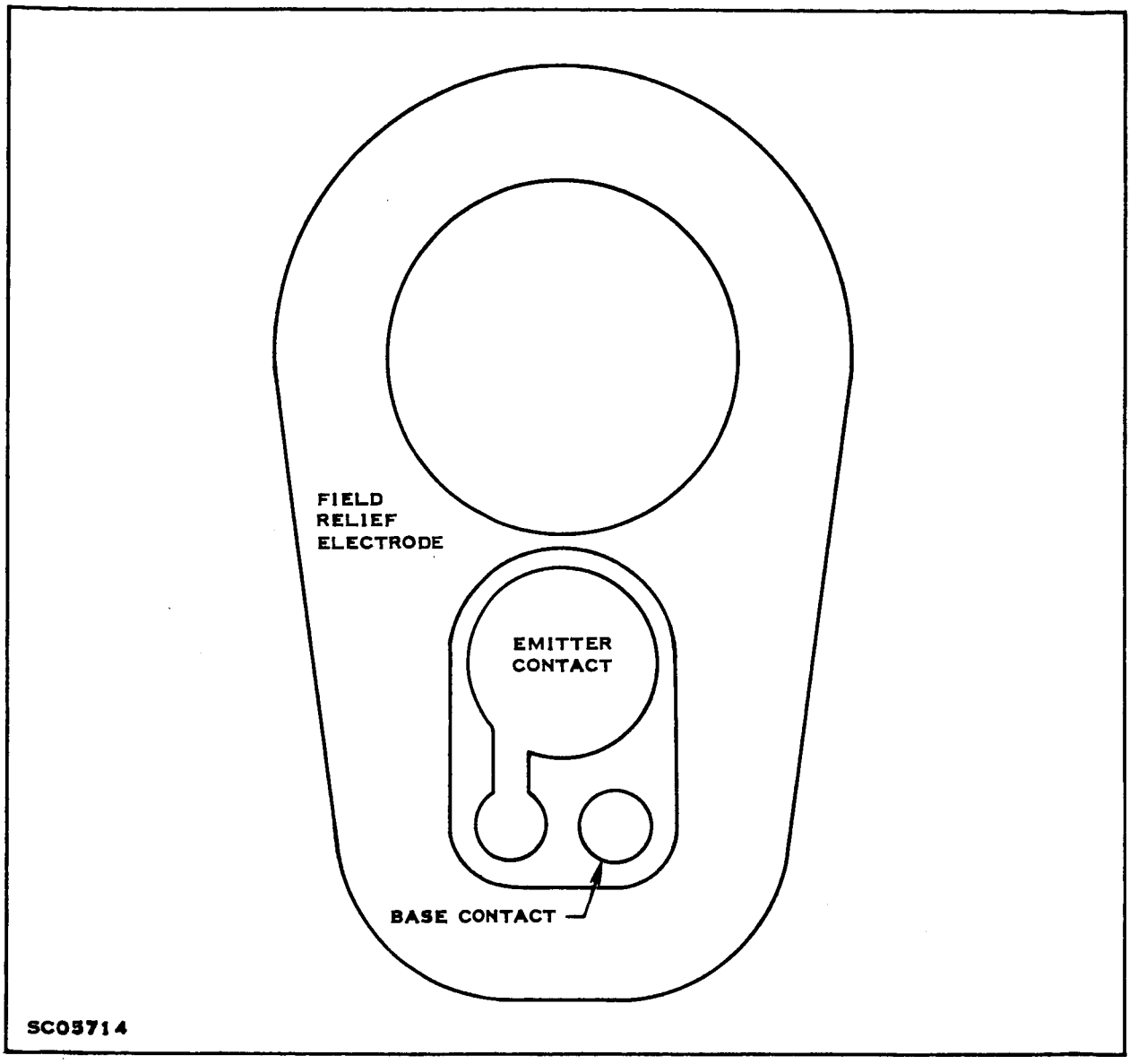

Figure 5. Metallization Layout

SECTION III

CONCLUSIONS AND RECOMMENDATIONS

Phototransistors satisfying the major requirements of current gain and breakdown voltage have been fabricated. An inversion layer effect which results in excessive high temperature leakage has developed in the transistor, but this should be eliminated with modifications being incorporated.

Gallium Arsenide Switches, which combine the Si phototransistor with a GaAs photon-emitting diode, demonstrate the desired optical-coupling and electrical characteristics.

SECTION IV

LITERATURE CITED

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2. "Integrated Electronic Gating System For Multiplexing Applications," IBM, JPL Contract No. 950492, December 15, 1964.

3. Texas Instruments Incorporated, "Photon-Coupled Isolation Switch," JPL Contract No. 951340, First Quarterly Progress Report, 1 January to 31 March 1966.